

REMARKS

Claims 1 - 11 remain pending in this application, of which claim 1 has been amended. No new matter has been added. Applicant respectfully submits that this Amendment is fully responsive to the Office Action dated **January 29, 2003**.

Examiner Interview

The courtesies extended by Examiner Lewis and Supervisory Examiner Whitehead during the May 8, 2003 interview are gratefully appreciated. The substance of the interview is incorporated into the following remarks.

35 U.S.C. §112, Second Paragraph, Rejection:

Claims 1 - 11 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

This rejection is respectfully traversed.

Applicant respectfully submit that the amendments to claim 1 obviates the rejection of claims 1 - 11 under 35 U.S.C. §112, second paragraph. Moreover, it is respectfully submitted that during the May 8, 2003 interview it was agreed to that claim 1, as amended, overcomes this rejection. Accordingly, withdrawal of the rejection of claims 1 - 11 under 35 U.S.C. §112, second paragraph,

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is respectfully solicited.

As To The Merits:

As to the merits of this case, the Examiner maintains the following rejections:

1) claims 1-5, 7, 8 and 11 stand rejected under 35 U.S.C. §103(a) as being obvious over Saito (U.S. Patent No. 5,773,853) in view of Applicant's prior art Figs. 1 and 2;

2) claim 6 stands rejected under 35 U.S.C. §103(a) as being obvious over Saito in view of Applicant's prior art Figs. 1 and 2 and Nakanishi (U.S. Patent No. 5,477,066); and

3) claims 9 and 10 stand rejected under 35 U.S.C. §103(a) as being obvious over Saito in view of Applicant's prior art Figs. 1 and 2 in view of Kuroda et al. (U.S. Patent No. 5,837,565).

Each of these rejections is respectfully traversed.

During the May 8, 2003 interview, it was explained that the present claimed invention calls for a graded channel layer which includes a second compound semiconductor layer of which one constituent element of said second compound semiconductor layer has a peak distribution in the inside of said channel layer in a thickness direction.

For example, as illustrated in Fig. 4A of the present application, the Indium composition ratio has a peak distribution in the inside of the second compound semiconductor in the channel layer 3 in a thickness direction. Therefore, even if the fluctuation of the gate voltage or the reduction of the gate voltage, etc is caused, the steep increase/decrease of the carrier density in the channel layer is suppressed and the mutual conductance that is higher and more stable than in the prior art is obtained.

In contrast, in Saito ('853), the InGaAs layer 23 and GaAs layer 24 are grown in alternate layers to form GaAs/InGaAs layer 25 for which each alternating InGaAs layer 23 may have a step increase of its InAs composition.

In other words, Saito is silent with regard to a single InGaAs layer 23 having a peak distribution. Instead, Saito discloses that each individual InGaAs layer 23 has a constant InAs composition ratio, although each alternately layer 23 may have an increased Indium composition to thereby reduce the thickness as illustrated in Fig. 5 of Saito.

Thus, it is only described in Saito to increase the composition ratio y of the buffer layer from the lower side to upper side sequentially, and it is not described and suggested such that a peak of a distribution of one constituent element (In) exists in the inside of the graded channel layer in a thickness direction.

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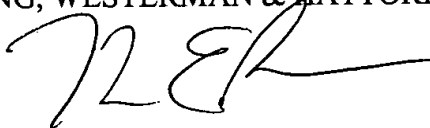
If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made

IN THE CLAIMS:

Claim 1 has been **AMENDED** to read as follows:

1. (Thrice amended) A compound semiconductor device comprising:

a substrate formed of a first compound semiconductor;

a buffer layer formed on the substrate;

a graded channel layer formed on the buffer layer, said graded channel layer composed [and formed] of a second compound semiconductor layer doped with an impurity of which one constituent element of said second compound semiconductor layer has a peak distribution in the inside of said graded channel layer in a thickness direction, thereby an energy band gap of the graded channel layer is made narrower in the inside than at both ends in the thickness direction [an energy band gap is made narrower inside than both ends by making a peak of distribution of one constituent element exist in the inside except the both ends in a thickness direction and doped with an impurity];

a barrier layer formed on the graded channel layer;

a gate electrode formed on the barrier layer to come into Schottky-contact with the barrier layer; and

a source electrode and a drain electrode formed on both sides of the gate electrode to flow a current into the graded channel layer via the barrier layer.